or later during prosecution.

Attached hereto is a marked-up version of the changes made to the specification and/or claims by the current Amendment. The attached page is captioned "**VERSIONS WITH MARKINGS TO SHOW CHANGES MADE**".

I. THE CLAIMED INVENTION

Applicant's invention, as disclosed and claimed, for example by independent claim 1, is directed to a semiconductor device. The semiconductor device includes a semiconductor chip, a chip-mounting substrate which is provided with the semiconductor chip mounted on a top surface thereof and first conductive pads formed on a bottom surface thereof and connected with the semiconductor chip electrically, solder balls formed on the first conductive pads, a printed circuit board on which second conductive pads connected with the solder balls are formed, and material injected into a clearance formed between the chip-mounting substrate and the printed circuit board. Uneven roughness is formed on a surface which is brought into contact with the material of at least one of the chip-mounting substrate and the printed circuit board. (See Page 15, lines 1-4; Page 16, lines 13-19; and Page 17, lines 3-9).

A key feature is an uneven roughness on a surface which increases the contact area of the rough surface promoting greater adhesive strength with a separate surface (e.g., a chip-mounting substrate and a printed circuit board according to claim 1). (See Page 4, line 17 through Page 5, line 4; and Page 15, line 23-Page 16, line 4). A very similar feature in a similar embodiment of a semiconductor device, as disclosed and claimed, for example by independent claim 4, is at least one of the lead frame and the printed circuit board is provided with uneven rough contact surfaces in direct contact therebetween." (See Page 20, lines 23-

25; Page 21, lines 21-24and

As a result of this inventive structure, including an uneven roughness on a surface, exfoliation is reduced between adhered surfaces, which increases the reliability of the semiconductor device operating in the electronic circuit.

II. THE PRIOR ART REJECTION

A. The § 103(a) Rejection Based on the Prior Art in View of Enomoto et al.

The Office Action alleges that the Prior Art and Enomoto et al. ("Enomoto") would have been combined to form the claimed invention, and thus claims 1-3 are rejected as being unpatentable.

First, Applicant agrees, in part, with the Office Action that the Prior Art "does not disclose uneven[ness] roughness being formed on a surface of a semiconductor chip mounted on a [the] printed circuit board." An important structural feature of Applicant's invention.

Second, Applicant asserts that it would not have been obvious to combine these references and even if combined, the combination would not teach or suggest each and every element of the claimed invention with an uneven roughness formed on a surface. Based on this structural feature, Applicant's invention increases the contact area of the rough surface promoting greater adhesive strength with a separate surface, e.g., between the printed circuit board and the chip mounting substrate, which reduces exfoliation between adhered surfaces, thereby increasing the reliability of the semiconductor device operating in the electronic circuit.

Enomoto like the Prior Art fails to disclose the structural features of Applicant's invention. Enomoto discloses an adhesive for electroless plating, printed circuit boards and method of fabricating the same, in which the adhesion property between a printed circuit

board pattern is improved. Enomoto further discloses an adhesive for electroless plating formed by dispersing particular heat-resistant granules easily soluble in an oxidizing agent into a particular heat resistant resin sparingly soluble in the oxidizing agent through a curing treatment. A printed circuit board is manufactured by using such an adhesive. (Enomoto at Abstract; Column 2, lines 38-49).

Enomoto further discloses obtaining a printed circuit board by forming electroless plated conductor circuit pattern onto an adhesive layer made from a heat-resistant resin where recesses are produced for the formation of an anchor on the electroless plated film by chemically etching and dissolving out and removing portions of the heat resistant particles through an oxidizing agent (See Column 3, lines 14-25; and Figure 1b, part 4(a)). The heat resistant particles, which are oxidized and removed, to form the recesses are an average particle size of 2-10 μm. (See Column 3, lines 9-12). The recesses of a specific size range formed in the electroless plated film are structurally different than Applicant's uneven roughness on a surface without reference to any size range formed by mechanical grinding. Based on this structural difference, Enomoto does not teach or suggest Applicant's invention.

Finally, in addition to the structural deficiencies of the Enomoto and the Prior Art, the references separately, or in combination, fail to teach, disclose or provide a motivation for being combined. In particular, Enomoto's primary purpose is to solve the drawbacks in the adhesive for electroless plating in producing the printed circuit boards, and thus improve the adhesion property between a printed circuit board and the semiconductor chip-mounting substrate. The Prior Art, however, pertains to semiconductor chips, which are attached to printed circuit boards, not producing printed circuit boards, and the Prior Art also does not disclose, teach or suggest improving surface bonding by any means. (See Column 2, lines 39-48; and Page 2, line 25 through Page 3, line 21). According, Applicant strongly asserts that

these structural differences and objectives provide no motivation for being combined and the Office Action provides no motivation to combine other than to assert that it would be obvious to one having ordinary skill in the art at the time.

Therefore, Applicant's invention is patentable over this combination.

Finally, regarding the dependent claims 2-3, which depend from claim 1, these claims are patentable not only by virtue of their dependency from the independent claim but also by the additional limitations they recite.

For the reasons stated above, the claimed invention is fully patentable over the cited references.

B. The § 103(a) Rejection Based on Kweon et al. in View of Sakuma et al.

The Office Action alleges that Kweon et al. ("Kweon") and Sakuma et al. ("Sakuma") would have been combined to form the claimed invention, and thus claim 4 is rejected as being unpatentable.

First, Applicant agrees with the Office Action that Kweon "does not disclose at least one of the lead frame and the printed circuit board with uneven[ness] roughness at contact surfaces in direct contact therebetween." Important structural features of Applicant's invention.

Second, Applicant asserts that it would not have been obvious to combine these references and even if combined, the combination would not teach or suggest each and every element of the claimed invention with an uneven roughness at contact surfaces in direct contact. Based on these structural features, Applicant's invention increases the contact area of the rough surface promoting greater adhesive strength with a separate surface, which reduces exfoliation between adhered surfaces, thereby increasing the reliability of the semiconductor device operating in the electronic circuit.

Sakuma like Kweon fails to disclose the structural features of Applicant's invention. Sakuma relates to the mounting of a semiconductor silicon chip and discloses a circuit substrate for use in manufacturing integrated circuit devices by the strip-support method in connection with a semiconductor element having conductive pads. The circuit substrate includes a base layer and a conductive circuit layer supported on the base layer for mechanically and electrically coupling to the conductive pads of a semiconductor device. The conductive circuit layer includes a plurality of finger leads with a bump at the end of each finger lead for mechanically and electrically coupling to one of the conductive pads. The coupling surface of each bump has a roughness in a range between 5 and 20 microns. The inherent roughness of the bumps can be augmented by plating bumps with nickel and gold. A method for forming bumps on the conductive layer of a circuit substrate for attachment of the circuit substrate to conductive pads of a semiconductor element is also provided. The method includes coating a front and back surface of the conductive layer with photo-resists. Then the photo-resists on both surfaces of the conductive layer are patterned by simultaneous exposure and development. Next, both surfaces of the conductive layer are half-etched. Then, one of the surfaces of the conductive layer is coated with a protective resist and the other surface of the conductive layer is etched. Finally, the photo-resist and protective resist are removed. (Sakuma at Abstract).

Sakuma, in particular, discloses, in part, a circuit substrate structure 100 with a bump 6 of a finger lead 4 with a contact surface 7 of the bump 6. The "[b]ump region 6 is formed of copper foil 16, nickel layer 18 and gold layer 19. Plating layers 18 and 19 are thickest at the areas at which the electric current is concentrated, i.e., the outwardly extending projections 17 on surface 7 and thinner in the areas surrounding projecting portions 17. As a result, the overall roughness of surface 7 is increased." (See Column 7, lines 55-68).

"Accordingly, a range of roughness is between about 5 and 20 microns is desired and a roughness of the contact surface 7 of substrate bump 6 between 5 and 15 microns is most preferred." (See Column 6, lines 61-64). Further, under heat and pressure the contact surface 7 is brought into contact and coupled with a first positioning aluminum pad 10 of integrated circuit 9, this results in the rough projecting portions of connecting surface 7 of bump 6 being crushed with the aluminum oxide film on the surface of the aluminum pad 10 being destroyed. Consequently "the metal forming substrate bump 6 and aluminum pad 10 react easily to form an efficient alloy thereby providing a strong connection."(See Column 5, lines 44 - Column 6, lines 4; and Column 6, lines 29 - Column 7, lines 16). Therefore, Sakuma relates to the mounting of a semiconductor silicon chip.

In contrast, Applicant's invention does not intend to improve the chip mounting itself but improves an adhesive strength between the printed circuit board and the semiconductor chip-mounting substrate. Applicant's invention discloses "at least one of the lead frame and the printed circuit board is provided with uneven rough contact surfaces in direct contact there- between." The uneven rough contact surfaces is comprised of a single layer without reference to any size range formed by mechanical grinding whereas Sakuma, as discussed above, has a significantly different structural configuration where the bumps are multi-layer compositions of copper foil with a subsequent nickel layer and gold layer of a specific size range, 5-20 microns, formed at the end of a finger lead, which is part of a conductive layer of an integrated circuit device.

Applicant's invention further teaches "uneven rough contact surfaces in direct contact there between," which increases the area of the contact surface, whereas Sakuma discloses the formation of an alloy, i.e., an intermediate structure, whereby the contact surfaces are in indirect contact. Therefore, the Sakuma mechanism relies on the melting of compounds to

form an alloy, i.e, a binding material, to hold the contact surfaces in place and relates to the mounting of the semiconductor silicon chip as opposed to Applicant's invention with increased surface area to enhance binding without formation of an intermediate binding material, i.e., an alloy, to improve an adhesive strength between the printed circuit board and the semiconductor chip-mounting substrate. Based on these structural differences, Sakuma does not teach or suggest Applicant's invention.

Finally, in addition to the structural deficiencies of Sakuma and Kweon, the references separately, or in combination, fail to teach, disclose or provide a motivation for being combined. In particular, Sakumo's primary purpose relates to the mounting of a semiconductor silicon chip and to "provide an improved method for forming the bumps on the conductive layers of the circuit substrates where the positioning error of the bumps on the finger leads are prevented" and " provide a circuit substrate with bumps having a roughness of between 5 and 15 microns to improve connection of the circuit substrate structure to the conductive pad of the IC chip." (See Column 2, lines 60-66; Column 3, lines 41-46).

In contrast, Kweon's object is to improve the grounding property by the particular packaging structure not the improvement of adhesive strength like Applicant's invention. Kweon, in particular, pertains to semiconductors not IC chips and, more particularly, to "a packaging structure for a surface-mounting type semiconductor package, which allows a reduction of the noise, without deteriorating the operation speed or mounting density of the package." (See Column 3, lines 14-19). According, Applicant strongly asserts that these structural differences and objectives provide no motivation for being combined and the Office Action provides no motivation to combine other than to assert that it would be obvious to one having ordinary skill in the art at the time. Therefore, Applicant's invention is patentable over this combination.

For the reasons stated above, the claimed invention is fully patentable over the cited references.

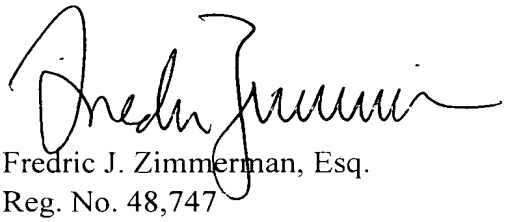
III. FORMAL MATTERS AND CONCLUSION

In view of the foregoing, Applicant submits that claims 1- 4 and 14-20, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,



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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the claims:

Claims 5-13 are canceled without prejudice or disclaimer.

The claims were amended as follows:

1. (Amended) A semiconductor device, comprising:

a semiconductor chip[,];

a chip-mounting substrate which is provided with said semiconductor chip mounted on a top surface thereof and first conductive pads formed on a bottom surface thereof and connected with said semiconductor chip electrically[,];

solder balls formed on said first conductive pads[,];

a printed circuit board on which second conductive pads connected with said solder balls are formed[,]; and

material injected into a clearance formed between said chip-mounting substrate and said printed circuit board,

wherein uneven roughness is formed on a surface which is brought into contact with said material of at least one of said chip-mounting substrate and said printed circuit board.

2. (Amended) A semiconductor device according to claim 1, wherein:

said uneven roughness is formed on said first conductive pads or on said second conductive pads selectively.

3. (Amended) A semiconductor device according to claim 1, wherein:

said uneven roughness is shaped into a slit-like configuration or into a dimple-like configuration.

4. (Amended) A semiconductor device, comprising:

a semiconductor chip[,];

a lead frame which is provided with said semiconductor chip mounted thereon and electrically connected with said semiconductor chip[,]; and

a printed circuit board including third conductive pads which are formed thereon and brought into direct contact with said lead frame,

wherein at least one of said lead frame and said printed circuit board is provided with uneven rough contact surfaces in direct contact therebetween.